Greenbank Electronics

USE OF MXD-2 WITH TINY BASIC V1.2

THE 'KEMITRON' MXD-2 CARD HAS LINKS WHICH CAN BE USED TO SET ITS ADDRESS TO ANY ONE OF THE FOUR 16-K BLOCKS IN THE TOTAL 64K AVAILABLE WITH A 16-BIT ADDRESS BUS. I.E., IF 4K PAGES (0-F) ARE CONSIDERED, THE MXD-2 RAM CAN BE LOCATED ON PAGES 0,1,2,3 OR 4,5,6,7 OR 8,9,A,B, OR C,D,E,F.

WHILST THIS ARRANGEMENT IS IDEAL FOR THE CP/M FLOPPY DISC SYSTEM, WHICH REQUIRES LARGE AMOUNTS OF CONTINUOUS RAM STARTING AT '0', THERE IS A POTENTIAL DIFFICULTY IF THE MXD-2 IS TO BE USED WITH SAY THE TINY BASIC PROGRAM VERSION V1.2 FOR THE Z80: THIS PROGRAM RESIDES IN ROM ON PAGE '0', AND REQUIRES CONTINUOUS RAM FROM PAGE '1' UPWARD. MANY USERS HAVE 8K OF RAM (ON THE MXA-3 CARD) LOCATED ON PAGES '1' AND '2', BUT IF THE UNMODIFIED MXD-2 IS PURCHASED FOR EXPANSION OF SUCH A SYSTEM THEN IT LEAVES PAGE '3' EMPTY IF IT STARTS ON THE LOWEST NON-'0' PAGE, (PAGE 4).

THE FOLLOWING SOLUTIONS TO THIS POTENTIAL PROBLEM HAVE BEEN PREPARED IN HASTE, WITH THE OBJECTS OF MINIMISING THE NUMBER OF EXTRA COMPONENTS REQUIRED, AND AMOUNT OF TRACKS TO BE CUT. THEY ARE THEREFORE NOT VERY 'PRETTY' CIRCUITS, SO WE WOULD VERY MUCH APPRECIATE IT IF ANY USER COULD LET US KNOW IF HE HAS FOUND A BETTER CIRCUIT.

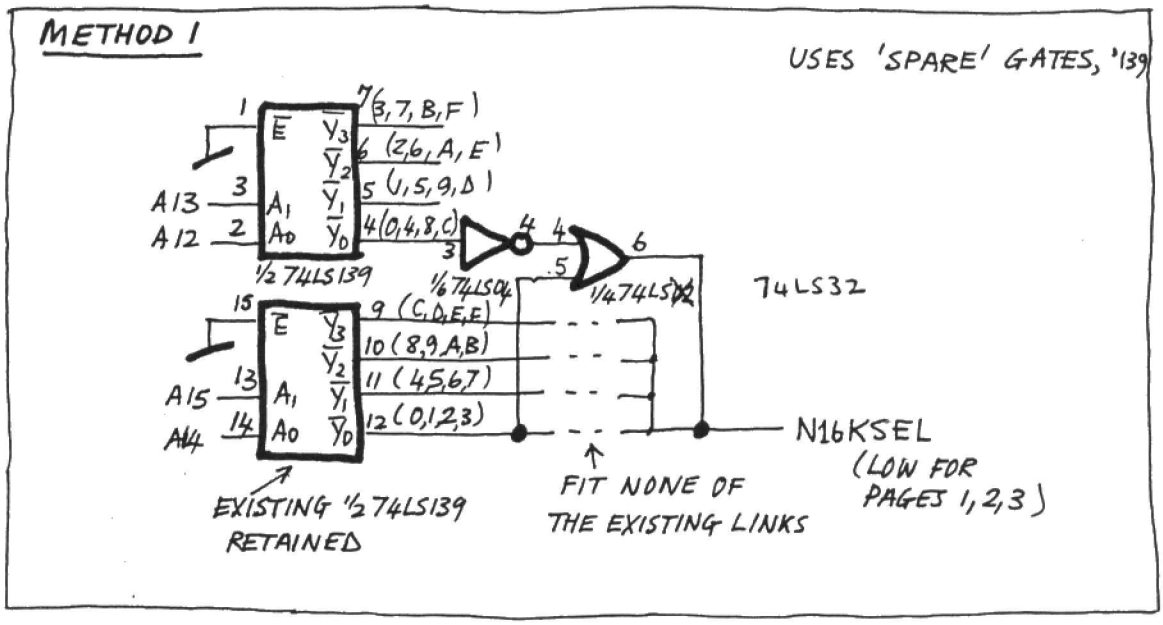
① METHOD 1 : MXD-2 ON PAGES 1, 2, 3 (I.E. NOT ON PAGE 0).

SINCE DYNAMIC RAM IS SO CHEAP, IT CAN OFTEN MAKE SENSE TO USE IT IN PLACE OF STATIC RAM, EVEN IF IT IS 25% UNUSED. IF 12K OF RAM IS SUFFICIENT ON THE MXD-2 CARD THEN IT CAN SIMPLY BE LOCATED IN THE FIRST 16K BLOCK, WITH PAGE '0' DISABLED TO ALLOW SYSTEM FIRMWARE STARTING AT '0'.

IF AN MXA-3 CARD IS AVAILABLE, THIS CAN SIMPLY BE RELOCATED TO PAGES 4,5 TO GIVE A TOTAL OF 12K+8K = 20K OF RAM.

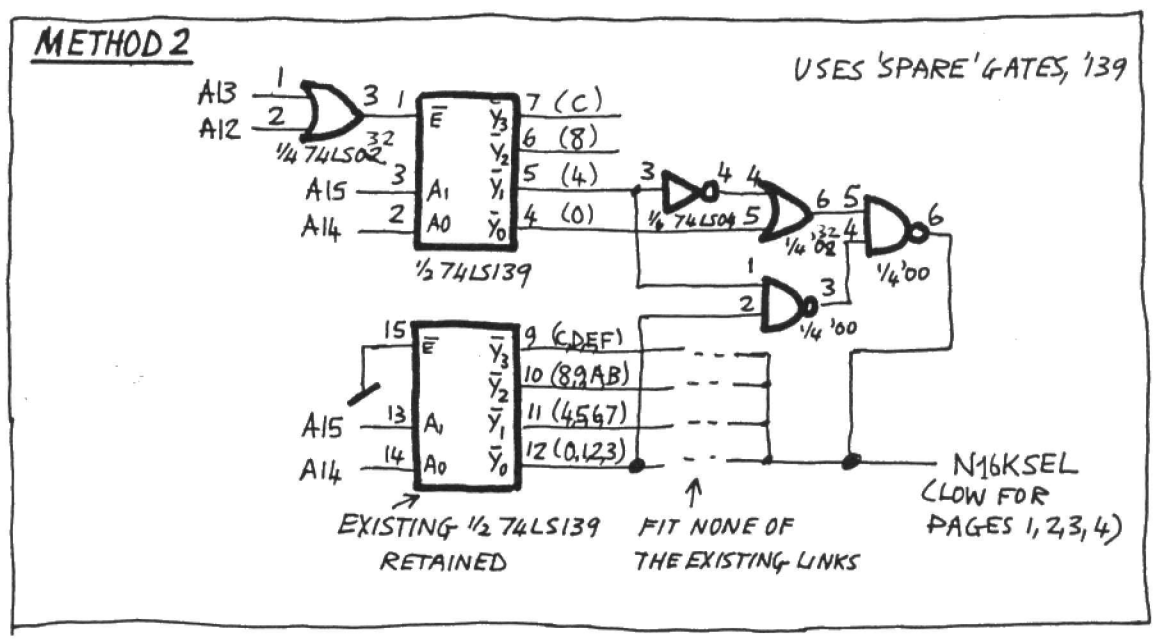
THE CIRCUIT DIAGRAM IS SHOWN ON THE NEXT PAGE. THE EXTRA IC SECTIONS USED ARE ALL TO BE FOUND AS SPARE PACKS ON THE MXD-2 BOARD, SO THIS LEAVES THE 'PATCH' AREA CLEAR FOR ANY SPECIAL PURPOSE THE USER MAY HAVE.

ROCK
GREENBANK ELECTRONICS, ~~82~~ 460 NEW CHESTER RD., ~~NEW~~ FERRY, ~~WIRRAL~~,
MERSEYSIDE. ~~L62 5AG.~~ L42 2AE. TEL: 051-645 3391



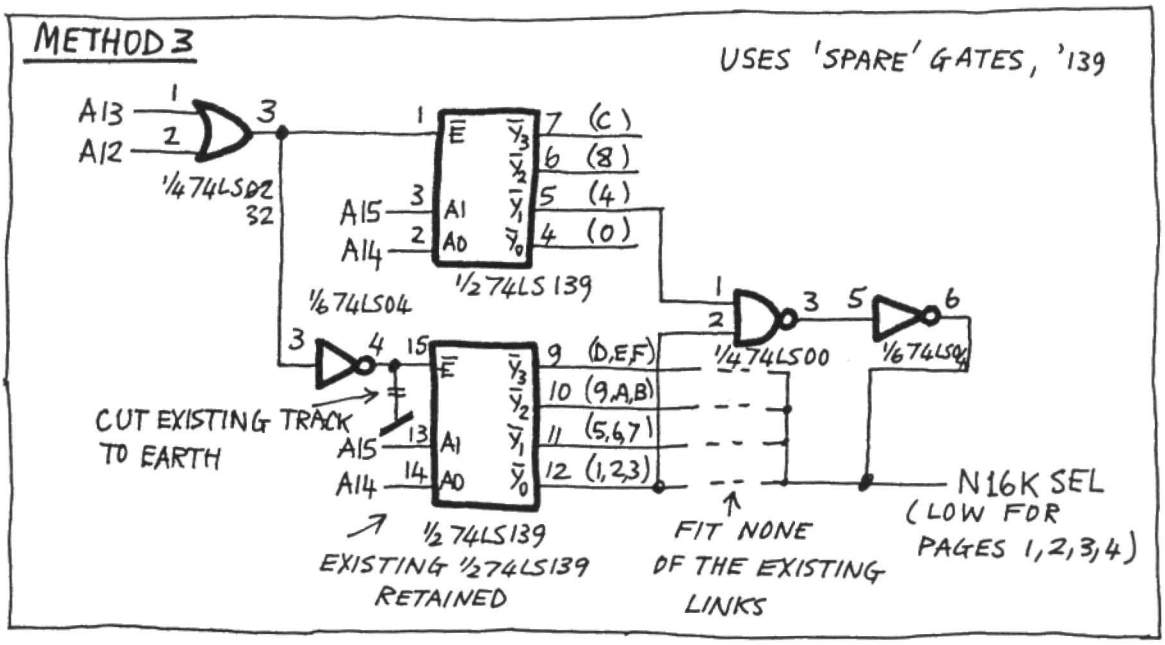
② METHOD 2 : MXD-2 ON PAGES 1, 2, 3, 4.

IF THE LOSS OF 25% OF THE AVAILABLE RAM ON THE MXD-2 BOARD AS DESCRIBED IN METHOD 1 IS UNACCEPTABLE THEN THE FOLLOWING METHOD CAN BE CONSIDERED. (AN MXA-3 BOARD IF USED, CAN BE RELOCATED TO PAGES 5, 6, GIVING A TOTAL OF 16K + 8K = 24K OF RAM)



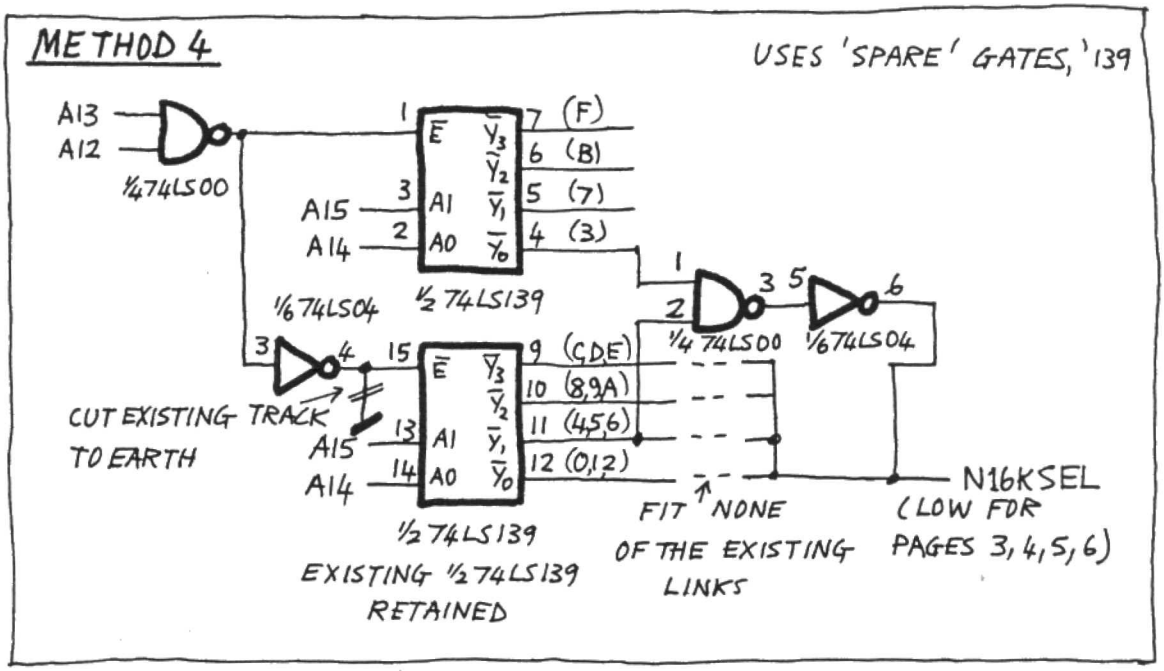
③ METHOD 3: MXD-2 ON PAGES 1, 2, 3, 4

THIS GIVES THE SAME RESULTS AS METHOD 2, BUT USES ONE LESS GATE. IT DOES HOWEVER INVOLVE A CUT IN THE COPPER TRACK (FROM PIN 15 OF THE 74LS139 TO EARTH), AND SO WE REALLY FAVOUR METHOD 2 OURSELVES.



(4) METHOD 4: MXD-2 ON PAGES 3,4,5,6.

IT IS SUGGESTED THAT THE MXD-2 BOARD BE BUILT AND TESTED BEFORE IT BECOMES THE TINY BASIC RAM STARTING AT PAGE 1, AS DESCRIBED IN METHODS 1-3. IF THE USER HAS A WORKING SYSTEM WITH AN MXA-3 8K STATIC RAM CARD WHICH IS LOCATED AT PAGES 1 AND 2, AND IT IS DESIRED TO LEAVE THIS ABSOLUTELY UNDISTURBED, THEN THE MXD-2 CAN BE REARRANGED TO OCCUPY PAGES 3, 4, 5, 6, AND NEED NOT BE TESTED IN ADVANCE.



ACCESS TIME.

ASSUMING A 10 NS WORST CASE PROPOGATION TIME THROUGH EACH OF THE EXTRA GATES ADDED, THE TIME TAKEN FROM VALID INPUT ADDRESSES TO THE 'N16KSEL' SIGNAL, IS INCREASED BY THE FOLLOWING AMOUNTS:

METHOD 1:	20 NS
METHOD 2:	40 NS
METHOD 3:	40 NS
METHOD 4:	40 NS

NORMALLY THIS WOULD MAKE A MEMORY CARD SLOWER BY THE SAME AMOUNT, BUT IT MUST BE REMEMBERED THAT MOST Z80 DYNAMIC MEMORY CARDS, INCLUDING THE MXD-2, BEGIN TIMING FROM THE NMREQ SIGNAL, NOT FROM VALID ADDRESS TIME.

THE Z80 TIMING IS SUCH THAT NMREQ IS ISSUED 205 NS AFTER VALID ADDRESS TIME AND SO THE EXTRA 20 OR 40 NS PROPOGATION DELAY IN THE GATES IN THE SUGGESTED CIRCUITS IS ABSORBED IN THE 205 NS WHEN THE CARD IS WAITING FOR NMREQ, AND SO IS OF NO CONSEQUENCE.

(THE 205 NS FIGURE ABOVE IS FOR A CPU CLOCK FREQUENCY OF 2·0 MHZ, WHICH IS OUR RECOMMENDATION TO SUIT THE MXD-2 CARD. USERS OF THE 4·0 MHZ FREQUENCY MAY BE INTERESTED TO KNOW THE CORRESPONDING FIGURE FOR THE ADDRESSES BEING STABLE PRIOR TO NMREQ IS 90 NS, AGAIN THE MODIFICATIONS SUGGESTED INVOLVE TOTAL DELAYS LESS THAN THIS FIGURE, AND SPEED IS UNAFFECTED).

D.M.P. 22-8-80